MPPS[™] Miniature Package Power Solutions DUAL 20V P-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

P-Channel V_{(BR)DSS} = -20V; $R_{DS(ON)}$ = 0.6 Ω ; I_D = -1.0A

DESCRIPTION

Packaged in the new innovative 3mm x 2mm MLP(Micro Leaded Package) outline this dual 30V N channel Trench MOSFET utilizes a unique structure combining the benefits of Low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage power management applications. Users will also gain several other **key benefits**:

Performance capability equivalent to much larger packages

Improved circuit efficiency & power levels

PCB area and device placement savings

Reduced component count

FEATURES

- Low On Resistance
- Fast switching speed
- · Low threshold
- Low gate drive
- 3mm x 2mm MLP

APPLICATIONS

- DC-DC Converters
- Power Management Functions
- Disconnection switches
- Motor Control

ORDERING INFORMATION

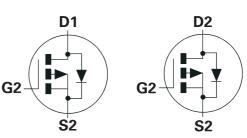
DEVICE	REEL	TAPE WIDTH	QUANTITY PER REEL
ZXMP62M832TA	7′′	8mm	3000 units

DEVICE MARKING

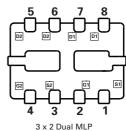
PROVISIONAL ISSUE A - MAY 2002



3mm x 2mm Dual Die MLP



PINOUT



underside view



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	P-Channel	UNIT
Drain-Source Voltage	V _{DSS}	-20	V
Gate-Source Voltage	V _{GS}	±12	V
Continuous Drain Current@V _{GS} =10V; T _A =25°C (b)(f)	ID	-1.6	A
@V _{GS} =10V; T _A =70°C (b)(f)		-1.3	A
@V _{GS} =10V; T _A =25°C (a)(f)		-1.3	A
Pulsed Drain Current	I _{DM}	-5.6	А
Continuous Source Current (Body Diode)(b)(f)	۱ _S	-2.7	А
Pulsed Source Current (Body Diode)	I _{SM}	-5.6	А
Power Dissipation at TA=25°C (a)(f)	P _D	1.5	W
Linear Derating Factor		12	mW/°C
Power Dissipation at TA=25°C (b)(f)	PD	2.45	W
Linear Derating Factor		19.6	mW/°C
Power Dissipation at TA=25°C (c)(f)	PD	1	W
Linear Derating Factor		8	mW/°C
Power Dissipation at TA=25°C (d)(f)	P _D	1.13	W
Linear Derating Factor		8	mW/°C
Power Dissipation at TA=25°C (d)(g)	PD	1.7	W
Linear Derating Factor		13.6	mW/°C
Power Dissipation at TA=25°C (e)(g)	P _D	3	W
Linear Derating Factor		24	mW/°C
Operating and Storage Temperature Range	T _i :T _{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)(f)	$R_{\theta JA}$	83.3	°C/W
Junction to Ambient (b)(f)	$R_{\theta JA}$	51	°C/W
Junction to Ambient (c)(f)	$R_{\theta JA}$	125	°C/W
Junction to Ambient (d)(f)	$R_{\theta JA}$	111	°C/W
Junction to Ambient (d)(g)	$R_{\theta JA}$	73.5	°C/W
Junction to Ambient (e)(g)	$R_{\theta JA}$	41.7	°C/W

Notes

(a) For a dual device surface mounted on 8 sq cm single sided 2oz copper on FR4 PCB, in still air conditions with all exposed pads attached. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.

(b) Measured at t<5 secs for a dual device surface mounted on 8 sq cm single sided 2oz copper on FR4 PCB, in still air conditions with all exposed pads attached. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.
(c) For a dual device surface mounted on 8 sq cm single sided 2oz copper on FR4 PCB, in still air conditions with minimal lead connections only.
(d) For a dual device surface mounted on 10 sq cm single sided 1oz copper on FR4 PCB, in still air conditions with all exposed pads attached attached. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.

(e) For a dual device surface mounted on 85 sq cm single sided 2oz copper on FR4 PCB, in still air conditions with all exposed pads attached attached. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.

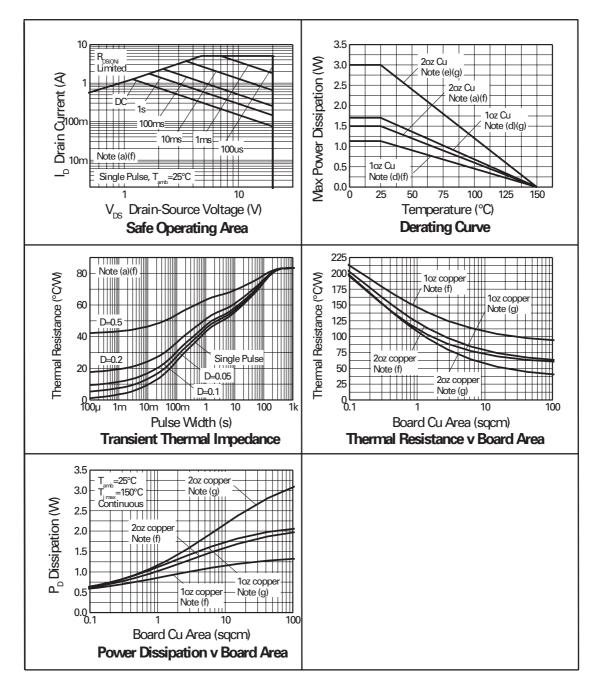
(f) For a dual device with one active die.

(g) For dual device with 2 active die running at equal power.

(h) Repetitive rating - pulse width limited by max junction temperature. Refer to Transient Thermal Impedance graph.

(i) The minimum copper dimensions required for mounting are no smaller than the exposed metal pads on the base if the device as shown in the package dimensions data. The thermal resistance for a dual device mounted on 1.5mm thick FR4 board using minimum copper 1 oz weight, 1mm wide tracks and one half of the device active is Rth = 250°C/W giving a power rating of Ptot = 500mW.





TYPICAL CHARACTERISTICS



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.	
STATIC							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	-20			V	I _D =-250μA, V _{GS} =0V	
Zero Gate Voltage Drain Current	I _{DSS}			-1	μA	V _{DS} =-20V, V _{GS} =0V	
Gate-Body Leakage	I _{GSS}			±100	nA	$V_{GS}=\pm 12V, V_{DS}=0V$	
Gate-Source Threshold Voltage	V _{GS(th)}	-0.7			V	$I_{D}^{=-250 \mu A}, V_{DS}^{=} V_{GS}$	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}			0.6 0.9	Ω Ω	V _{GS} =-4.5V, I _D =-0.61A V _{GS} =-2.7V, I _D =-0.31A	
Forward Transconductance (1)(3)	9fs	0.56			S	V _{DS} =-10V,I _D =-0.31A	
DYNAMIC (3)							
Input Capacitance	C _{iss}		150		pF		
Output Capacitance	Coss		70		pF	V _{DS} =-15V, V _{GS} =0V, f=1MHz	
Reverse Transfer Capacitance	C _{rss}		30		pF		
SWITCHING(2) (3)							
Turn-On Delay Time	t _{d(on)}		2.9		ns		
Rise Time	t _r		6.7		ns	$V_{DD} = -10V, I_{D} = -0.93A$	
Turn-Off Delay Time	t _{d(off)}		11.2		ns	$R_G=6.0\Omega$, $R_{D=11\Omega}$ (Refer to test circuit)	
Fall Time	t _f		10.2		ns]	
Total Gate Charge	0 _g		5.2	3.5	nC	V _{DS} =-16V,V _{GS} =-4.5V,	
Gate-Source Charge	Q _{gs}			0.5	nC	I _D =-0.61A	
Gate-Drain Charge	Q _{gd}			1.5	nC	(Refer to test circuit)	
SOURCE-DRAIN DIODE							
Diode Forward Voltage (1)	V _{SD}			-0.95	V	T _J =25°C, I _S =-0.61A, V _{GS} =0V	
Reverse Recovery Time (3)	t _{rr}		14.9		ns	T _J =25°C, I _F =-0.61A,	
Reverse Recovery Charge (3)	Q _{rr}		5.6		nC	di/dt= 100Å/µs	

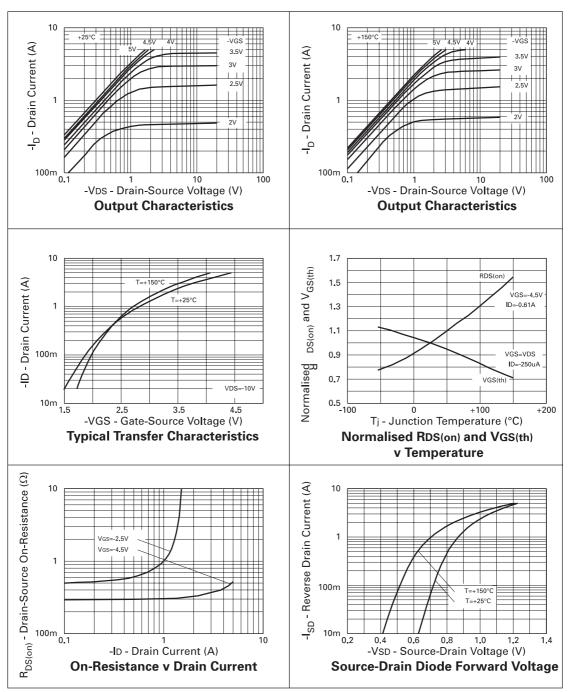
NOTES

(1) Measured under pulsed conditions. Width ${\leq}300\mu s.$ Duty cycle ${\leq}\,2\%$.

(2) Switching characteristics are independent of operating junction temperature.

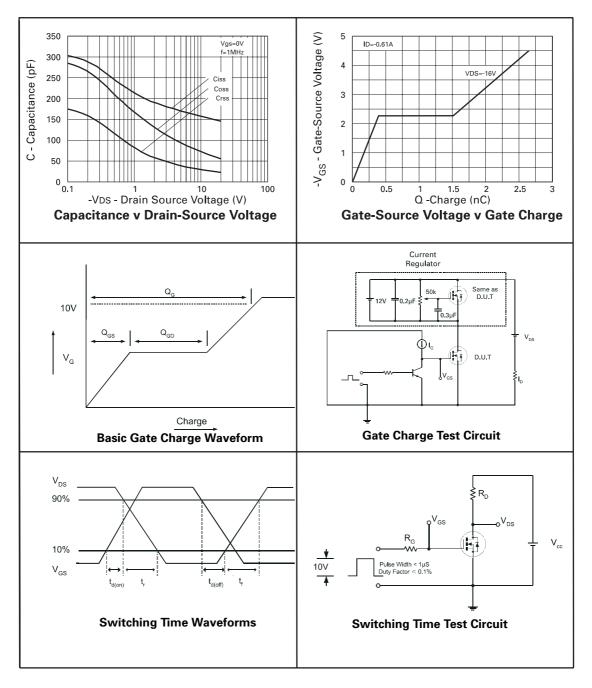
(3) For design aid only, not subject to production testing.





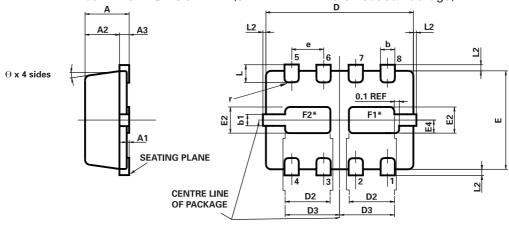
TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS





MLP832 PACKAGE OUTLINE (3mm x 2mm Micro Leaded Package)

*Exposed Flags. Solder connection to improve thermal dissipation is optional. F1 at collector 1 potential

F2 at collector 2 potential

CONTROLLING DIMENSIONS IN MILLIMETRES APPROX. CONVERTED DIMENSIONS IN INCHES

	MILLIN	IETRES	INC	HES		MILLIMETRES		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.	DIM	MIN.	MAX.	MIN.	MAX.
А	0.80	1.00	0.031	0.039	е	0.65 REF		0.0787 BSC	
A1	0.00	0.05	0.00	0.002	Е	2.00 BSC		0.0256 BSC	
A2	0.65	0.75	0.0255	0.0295	E2	0.43	0.63	0.017	0.0249
A3	0.15	0.25	0.006	0.0098	E4	0.16	0.36	0.006	0.014
b	0.24	0.34	0.009	0.013	L	0.20	0.45	0.0078	0.0157
b1	0.17	0.30	0.0066	0.0118	L2		0.125	0.00	0.005
D	3.00	BSC	0.118	BSC		0.075 BSC		0.0029 BSC	
D2	0.82	1.02	0.032	0.040	θ	0 °	12°	0 °	12°
D3	1.01	1.21	0.0397	0.0476					

MLP832 PACKAGE DIMENSIONS

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